

APPENDIX A.

A.1. Extension Connector Pin Description

A.1.1. Extension Connector for LCD/CRT/Touch Screen : J4

◆ 2mm-pitch, 44-Pin, Dip-type

Pin No.	Symbol	Description	Notes
1	R4	Red Data 4	
2	R5	Red Data 5	
3	R2	Red Data 2	
4	R3	Red Data 3	
5	R0	Red Data 0	
6	R1	Red Data 1	
7	PWREN	LCD Power Enable	
8	DGND	Ground	
9	G4	Green Data 4	
10	G5	Green Data 5	
11	G2	Green Data 2	
12	G3	Green Data 3	
13	G0	Green Data 0	
14	G1	Green Data 1	
15	END	End Signal for TFT LCD	
16	DGND	Ground	
17	B4	Blue Data 4	
18	B5	Blue Data 5	
19	B2	Blue Data 2	
20	B3	Blue Data 3	
21	B0	Blue Data 0	
22	B1	Blue Data 1	
23	N/C	–	
24	DGND	Ground	
25	HSYNC	Horizontal Sync Signal	
26	VSYNC	Vertical Sync Signal	

27	DGND	Ground	
28	DCLK	Data Input Clock	
29	N/C	–	
30	DE	Data Enable Signal	
31	VCC3.3	Power (3.3V)	
32	VCC3.3	Power (3.3V)	
33	VGA_R	Analog Red Signal (Optional)	
34	VGA_G	Analog Green Signal (Optional)	
35	VGA_B	Analog Blue Signal (Optional)	
36	LCD_VF0	Timing Signal for TFT LCD	
37	LCD_VF1	Timing Signal for TFT LCD	
38	LCD_VF2	Timing Signal for TFT LCD	
39	VD0	Video Data0 for STN LCD	
40	VD1	Video Data1 for STN LCD	
41	T_TOP	For 4-wired Resistive Touch Screen	
42	T_BOT		
43	T_RIGHT		
44	T_LEFT		

Table 1 J4 Pin Description

A.1.2. Extension Connector for PC104/ISA Bus : J5

◆ 2.54mm-pitch, 50-pin, Dip-type

Pin No.	Symbol	Description	Notes
1	VCC5.0	Power (5V)	
2	VCC3.3	Power (3.3V)	
3	LA0	Address Bus Signal	
4	D0	Data Bus Signal	
5	LA1	Address Bus Signal	
6	D1	Data Bus Signal	
7	LA2	Address Bus Signal	
8	D2	Data Bus Signal	
9	LA3	Address Bus Signal	
10	D3	Data Bus Signal	

11	LA4	Address Bus Signal	
12	D4	Data Bus Signal	
13	LA5	Address Bus Signal	
14	D5	Data Bus Signal	
15	LA6	Address Bus Signal	
16	D6	Data Bus Signal	
17	LA7	Address Bus Signal	
18	D7	Data Bus Signal	
19	LA8	Address Bus Signal	
20	D8	Data Bus Signal	
21	LA9	Address Bus Signal	
22	D9	Data Bus Signal	
23	LA10	Address Bus Signal	
24	D10	Data Bus Signal	
25	LA11	Address Bus Signal	
26	D11	Data Bus Signal	
27	LA12	Address Bus Signal	
28	D12	Data Bus Signal	
29	LA13	Address Bus Signal	
30	D13	Data Bus Signal	
31	LA14	Address Bus Signal	
32	D14	Data Bus Signal	
33	LA15	Address Bus Signal	
34	D15	Data Bus Signal	
35	LA16	Address Bus Signal	
36	nGCS3	Chip Select Pin3: 0x18000000–0x200000	Active Low
37	LA17	Address Bus Signal	
38	nGCS4	Chip Select Pin4 : 0x20000000–0x280000	Active Low
39	LA18	Address Bus Signal	
40	nGCS5	Chip Select Pin5 : 0x28000000–0x300000	Active Low
41	LA19	Address Bus Signal	
42	nOE	Memory, I/O Read Signal	Active Low
43	LA20	Address Bus Signal	
44	nWE	Memory, I/O Write Signal	Active Low
45	LA21	Address Bus Signal	

46	HDD_IOR	HDD, CF Read Signal	Active High
47	nWAIT	Memory, I/O Wait Signal	3-State
48	HDD_IOW	HDD, CF Write Signal	Active High
49	DGND	Ground	
50	DGND		

Table 2 J5 Pin Description

A.1.3. Extension Connector for Peripheral : J6

◆ 2.54mm-pitch, 50-pin, Dip-type

Pin No.	Symbol	Description	Notes
1	VCC5.0	Power (5V)	
2	VCC3.3	Power (3.3V)	
3	AIN0	Analog Input (0V-3.3V)	
4	AIN1		
5	AIN2		
6	AIN3		
7	AIN4		
8	AIN5		
9	AIN6		
10	AIN7		
11	A_LEFT	Audio Codec Analog Left Output	
12	A_RIGHT	Audio Codec Analog Right Output	
13	VCC_RTC	Power for Real Time Clock (1.8V)	
14	VCC12.0	Power (12V)	Reserved
15	IIC_SCL	IIC Shift Clock Output	
16	IIC_SDA	IIC Shift Data	
17	nSS0	SPI Chip Select Signal	
18	nSS1		
19	SPICLK0	SPI Clock Signal	
20	SPICLK1		
21	SPIMISO0	SPI Master Input Slave Output	
22	SPIMISO1		
23	SPIMOSI0	SPI Master Output Slave Input	

24	SPIMOSI1		
25	UCLK	External Clock Input for UART	
26	nRST	Reset Signal for ARM	
27	UART_TXD0	UART0 Transmit Signal	
28	UART_RXD0	UART0 Receive Signal	
29	UART_TXD1	UART1 Transmit Signal	
30	UART_RXD1	UART1 Receive Signal	
31	UART_TXD2	UART2 Transmit Signal	
32	UART_RXD2	UART2 Receive Signal	
33	DI0	Digital Input Signal : Supports internal pull-up register & interrupt	
34	DO0	Digital Output Signal	
35	DI1	Digital Input Signal : Supports internal pull-up register & interrupt	
36	DO1	Digital Output Signal	
37	DI2	Digital Input Signal : Supports internal pull-up register & interrupt	
38	DO2	Digital Output Signal	
39	DI3	Digital Input Signal : Supports internal pull-up register & interrupt	
40	DO3	Digital Output Signal	
41	DI4	Digital Input Signal : Supports internal pull-up register & interrupt	
42	DO4	Digital Output Signal	
43	DI5	Digital Input Signal : Supports internal pull-up register & interrupt	
44	DO5	Digital Output Signal	
45	DI6	Digital Input Signal : Supports internal pull-up register	

		& interrupt	
46	DO6	Digital Output Signal	
47	DI7	Digital Input Signal : Supports internal pull-up register & interrupt	
48	DO7	Digital Output Signal	
49	DGND	Ground	
50	DGND		

Table 3 J6 Pin Description

A.1.4. IDE Connector for HDD/CDROM : J10

◆ 2mm-pitch, 44-pin, Dip-type

Pin No.	Symbol	Description	Notes
1	HDD_nRESET	Reset Signal for HDD	
2	DGND	Ground	
3	HD7	Data Bus Signal	
4	HD8		
5	HD6		
6	HD9		
7	HD5		
8	HD10		
9	HD4		
10	HD11		
11	HD3		
12	HD12		
13	HD2		
14	HD13		
15	HD1		
16	HD14		
17	HD0		
18	HD15		
19	DGND	Ground	
20	N/C	–	
21	HDD_DRQ	DMA Request Signal	

22	DGND	Ground	
23	HDD_IOW	HDD, I/O Write Signal	
24	DGND	Ground	
25	HDD_IOR	HDD, I/O Read Signal	
26	DGND	Ground	
27	HDD_nWAIT	HDD, Wait Signal	
28	N/C	–	
29	HDD_DACK	DMA Acknowledge Signal	
30	DGND	Ground	
31	HDD_INT	HDD, Interrupt Request Signal	
32	N/C	–	
33	HA1	HDD, Address Bus Signal 1	
34	N/C	–	
35	HA0	HDD, Address Bus Signal 0	
36	HA2	HDD, Address Bus Signal 2	
37	HDD_nCS0	HDD, Chip Select Signal	
38	HDD_nCS1		
39	N/C	–	
40	DGND	Ground	
41	VCC5.0	Power (5V)	
42	VCC5.0		
43	DGND	Ground	
44	N/C	–	

Table 4 J10 Pin Description

A.1.5. Extension Connector for JTAG Interface : CON1

- ◆ 2.54mm-pitch, 12-pin, Dip-type
- ◆ You need JTAG Adapter with 14-pin or 20-pin for JTAG Tools – Contact Us!

Pin No.	Symbol	Description	Notes
1	VCC3.3	Power (3.3V)	
2	TDI	TAP Controller Data Input for ARM	
3	CPLD_TDI	TAP Controller Data Input for CPLD	
4	TCLK	TAP Controller Clock for ARM	
5	CPLD_TCK	TAP Controller Clock for CPLD	

6	TMS	TAP Controller Mode Select for ARM	
7	CPLD_TMS	TAP Controller Mode Select for CPLD	
8	TDO	TAP Controller Data Output for ARM	
9	CPLD_TDO	TAP Controller Data Output for CPLD	
10	nTRST	TAP Controller Reset for ARM	
11	DGND	Ground	
12	HDD_nRESET	Reset Output Signal	

Table 5 CON1 Pin Description

A.2. LayOut

